	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	4	(high adj intensity) same (detect$3 near3 ((short adj circuit) (open adj circuit)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 08:53	
2	BRS	L3	4	2 and 315/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 08:54	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
3	BRS	L2	56	(high adj intensity) and (detect$3 near3 ((short adj circuit) (open adj circuit)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 08:54	
4	BRS	L6	117242	(variable varying varie$ alter$3) near4 frequency	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 09:32	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L7	9377	6 with (inverter converter)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 09:33	
6	BRS	L8	97	7 and (high adj intensity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 09:34	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
7	BRS	L9	50	8 and 315/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 10:56	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	3979	ignit$3 near3 capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:15	
2	BRS	L2	158	1 and (high adj intensity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:15	

should search again.

ignition capacitor feature may be novel

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
3	BRS	L3	747	ignit$3 adj capacitor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:15	
4	BRS	L4	37	3 and (high adj intensity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:15	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	23	4 and 315/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:18	
6	BRS	L6	17	5 and resonan$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 17:18	

	Error Definition	Errors
5		0
6		0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	2850	(disabl$3 ((shut$4 adj off) (shut$4 adj down))) near3 (inverter ballast)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 15:07	
2	BRS	L2	472	1 same (start$3 ignit$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 15:07	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
3	BRS	L3	37	2 and (high adj intensity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 16:16	
4	BRS	L5	24	3 and resonan$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/14 16:21	

	Error Definition	Errors
3		0
4		0

ADVANTAGE - Failsafe control for discharge lamp.

ABSTRACTED-PUB-NO: US 6002215A

EQUIVALENT-ABSTRACTS:

The discharge lamp, for a vehicle, is powered by a DC-AC converter (3) driven by a DC control circuit (6). A monitoring circuit (4) measures the lamp current or lamp voltage during the switching cycle and from the measured values derives a short circuit current, or a leakage current. If the leakage is above a set level, or if a short circuit is detected, a shut-down signal is generated to switch off the lamp.

The shut-down control is inhibited if there is a voltage fluctuation in the supply voltage. The shut-down control prevents undue overheating through leakage tracks e.g. if there is a series short through moisture.

USE - High intensity headlamp for vehicle.

ADVANTAGE - Failsafe control for discharge lamp.

CHOSEN-DRAWING: Dwg.1/12

TITLE-TERMS: CONTROL CIRCUIT DISCHARGE LAMP MONITOR CIRCUIT DETECT SHORT CIRCUIT LEAK CURRENT LAMP ACTIVATE SHUT=DOWN

DERWENT-CLASS: Q71 X26

EPI-CODES: X26-C01X;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1999-008172

7) The third exemplary embodiment of the invention represented in FIG. 3 has a mains voltage input with the mains voltage terminals j30, j31, a filter and a mains voltage rectifier GL3, a step-up convertor HS3 connected downstream, an intermediate circuit capacitor C30, which is connected to the output of the step-up convertor HS3 and supplies the supply voltage for an invertor HW3. Connected downstream of the invertor HW3 is a load circuit which is designed as a resonant circuit and has the resonance inductor L30, the capacitors C31, C32 and two electrical terminals j32, j33 for the at least one induction coil L31 of an electrodeless discharge lamp LP3. The invertor HW3 is driven with the aid of a control circuit S3. The ignition capacitor C31 is connected in parallel with the terminals j32, j33. One terminal of the balancing capacitor C32 is connected to the invertor HW3, while the other terminal of the balancing capacitor C32 is connected via the tap V30 to the resonance inductor L30. This circuit arrangement additionally has a non-reactive resistor R30, which is connected to the positive pole of the intermediate circuit capacitor C30, on the one hand, and to the tap V30 in the load circuit, on the other hand. The tap V30 is furthermore connected to an input of the control circuit S3. The control circuit S3 has a monitoring element which is connected upstream or integrated into the control circuit, said monitoring element being, for example, a logic circuit which monitors the electrical potential at the tap V30 and forwards a corresponding evaluation signal to the control unit S3. If no lamp LP3 is connected to the terminals j32, j33, then the tap V30 is at a comparatively high electrical potential essentially determined by the charge state of the intermediate circuit capacitor C30. If, on the other hand, at least one lamp LP3 is connected to the terminals j32, j33, then the tap V30 is connected to earth via the resonance inductor L30 and the induction coil L31 and the tap V30 is therefore at a comparatively low electrical potential. The monitoring element generates a digital or analogue evaluation signal corresponding to the electrical potential at the tap V30 and feeds said signal to the control circuit S3. The control circuit S3 is designed in such a way that it enables the invertor HW3 to start oscillating only when the electrical potential at the tap V30 falls below a predetermined value prescribed by the dimensioning of the circuit components. This ensures that no ignition attempts are made in the absence of a lamp LP3.

(8) The fourth exemplary embodiment of the invention represented in FIG. 4 has a mains voltage input with the mains voltage terminals j40, j41, a filter and a mains voltage rectifier GL4, a step-up converter HS4 connected downstream, an intermediate circuit capacitor C40, which is connected to the output of the step-up converter HS4 and supplies the supply voltage for an invertor HW4. Connected downstream of the invertor HW4 is a load circuit which is designed as a resonant circuit and has the resonance inductor L40, the capacitors C41, C42 and two electrical terminals j42, j43 for the at least one induction coil L41 of an electrodeless discharge lamp LP4. The invertor HW4 is driven with the aid of a control circuit S4. The ignition capacitor C41 is connected in parallel with the terminals j42, j43. One terminal of the balancing capacitor C42 is connected to the invertor HW4, while the other terminal of the balancing capacitor C42 is connected via the tap V40 to the resonance inductor L40. The tap V40 is furthermore connected to an input of the control circuit S4. This circuit arrangement additionally has a non-reactive resistor R40, which is connected to the positive pole of the intermediate circuit capacitor C40, on the one hand, and to a tap between the resonance inductor L40 and the terminal j42 in the load circuit, on the other hand. The control circuit S4 monitors the electrical potential at the tap V40. If no lamp LP4 is connected to the terminals j42, j43, then the tap V40 is at a comparatively high electrical potential essentially determined by the charge state of the intermediate circuit capacitor C40. If, on the other hand, at least one lamp LP4 is connected to the terminals j42, j43, then the tap V40 is connected to earth via the induction coil L41 and the tap V40 is therefore at a comparatively low electrical potential. The control circuit S4 has a monitoring element which is connected upstream or integrated into the control circuit, said monitoring element being, for example, a logic circuit which monitors the electrical potential at the tap V40 and generates a corresponding digital or analogue evaluation signal and feeds it to the control unit S4. The control circuit S4 is designed in such a way that it enables the invertor HW4 to start oscillating only when the electrical potential at the tap V40 falls below a predetermined value prescribed by the dimensioning of the circuit components. This ensures that no ignition attempts are made in the absence of a lamp LP4.

(9) The invention is not restricted to the exemplary embodiments explained in more detail above. By way of example, it is possible for the invention not just to be applied to externally controlled half-bridge invertors, rather it can also be applied to other voltage invertors such as, for example, full-bridge invertors or free-running half-bridge invertors.

(10) The circuit arrangement of the fifth exemplary embodiment as represented in FIG. 5 shows the application of the invention to a full-bridge invertor. The circuit arrangement according to the fifth exemplary embodiment has, in a manner similar to that described for the first exemplary embodiment, a mains voltage connection, a filter and a mains voltage rectifier and also a step-up converter, which are not represented in FIG. 5. The terminals j50, j51 shown in FIG. 5 are connected to the output of the step-up converter, with the result that the intermediate circuit capacitor C50 is connected in parallel with the output of the step-up converter. A full-bridge invertor comprising the switching transistors Q1, Q2, Q3, Q4 and a control circuit (not represented) is connected downstream of the intermediate circuit capacitor C50. A resonance inductor L50, an ignition capacitor C51 and a balancing capacitor C52 are arranged in the bridge path of the full-bridge invertor Q1, Q2, Q3, Q4. Two electrical terminals j52, j53 are connected in parallel with the ignition capacitor C51 and serve for the connection of at least one induction coil L51 of an electrodeless discharge lamp LP5. Furthermore, the circuit arrangement has a non-reactive resistor R50, which is connected to the positive pole of the intermediate circuit capacitor C50, on the one hand, and to a tap in the bridge path, on the other hand, and a current lead j54, which connects the control circuit (not represented) of the full-bridge invertor Q1, Q2, Q3, Q4 to a further tap in the bridge path. A DC path is produced in this way, into which are connected, proceeding from the positive pole of the intermediate circuit capacitor C50, the non-reactive resistor R50, the resonance inductor L50, the terminal j52, the induction coil L51 of the discharge lamp LP5, the terminal j53 and the current lead j54. This DC path is interrupted in the absence of a discharge lamp LP5. In that case, the control circuit, which, by way of example, may be designed as an integrated circuit in a manner similar to that in the first exemplary embodiment, receives no supply voltage and the full-bridge invertor Q1, Q2, Q3, Q4 cannot start to oscillate. The circuit arrangement does not, therefore, make any ignition attempts in the absence of a discharge lamp LP5.

(11) FIG. 6 shows the application of the invention to a free-running half-bridge invertor according to a sixth exemplary embodiment. This circuit arrangement has, in a manner similar to that described for the first exemplary embodiment, a mains voltage terminal, a filter and a mains voltage rectifier and also a step-up converter, which are not represented in FIG. 6. The terminals j60, j61 shown in Figure [lacuna] are connected to the output of the step-up converter, with the result that the intermediate circuit capacitor C60 is connected in parallel with the output of the step-up converter. A half-bridge invertor formed by the two switching transistors Q5, Q6 is connected downstream of the intermediate circuit capacitor C60. A load circuit which is designed as a resonant circuit and has a resonance inductor L60, an ignition capacitor C61, a balancing capacitor C62 and two electrical terminals j62, j63--arranged in parallel with the ignition capacitor C61--for at least one induction coil L61 of an electrodeless discharge lamp LP6 is connected to the centre tap between the two switching transistors Q5, Q6. This circuit arrangement additionally has a non-reactive resistor R60, which is connected to the positive pole of the intermediate circuit capacitor C60, on the one hand, and to a tap in the load circuit, on the other hand, for example to the centre tap between the two switching transistors Q5, Q6, and a current lead j64, which connects a second tap in the load circuit, said tap being located between the terminal j63 and the balancing capacitor, to an input of the control circuit (not represented) of the half-bridge invertor Q5, Q6. The control circuit of the half-bridge invertor Q5, Q6 comprises a transformer (not represented) having a primary winding connected into the load circuit of the half-bridge invertor and two secondary windings each connected to the control electrode of one of the two switching transistors Q5, Q6, and also a starting circuit which, with the aid of a diac, generates trigger pulses for the control electrode of the switching transistor Q6 in order to enable the half-bridge invertor to start oscillating. Such a free-running half-bridge invertor with such a control circuit is described for example in the German Patent Application with the official file reference 196 50 110.5.

(12) The current lead j64 is connected to the input of the starting circuit. In the absence of a discharge lamp LP6, the balancing capacitor C62 is charged only to an insufficient extent owing to its very large capacitance in comparison with the ignition capacitor C61, and the voltage drop across the balancing capacitor C62 is therefore comparatively small. Therefore, the starting circuit is supplied with voltage only to an insufficient extent via the current lead j64 in the absence of a discharge lamp LP6, with the result that the half-bridge invertor cannot start oscillating.

(13) FIGS. 7 to 13 show exemplary embodiments for circuit arrangements for operating two electrodeless discharge lamps in each case.

(14) The circuit arrangement according to the seventh exemplary embodiment as represented in FIG. 7 has a mains voltage input j70, j71, a filter circuit with a mains voltage rectifier GL7 connected downstream, said filter circuit being connected to the mains voltage input, a step-up converter HS7 connected to the DC voltage output of the rectifier GL7, an intermediate circuit capacitor C70 arranged in parallel with the output of the step-up converter HS7, and an externally controlled half-bridge invertor HW7, whose input is connected in parallel with the intermediate circuit capacitor C70. The half-bridge invertor HW7 is driven by means of an integrated circuit IC7, which receives its supply voltage via its terminals j72 and j73 and the resistors R70, R71 and R72. Two load circuits which are connected in parallel and are designed as resonant circuits are connected to the half-bridge invertor HW7, said load circuits each having a resonance inductor L72 and L73, respectively, a resonance capacitor C71 and C73, respectively, and also a further capacitor C72 and C74, respectively, and an electrodeless discharge lamp LP70 and LP71, respectively. The supply current for the integrated circuit IC7 flows via the two resonance inductors L72, L73 and via the induction coils L71 and L72 of the two electrodeless discharge lamps LP70, LP71. If one of the discharge lamps LP70 or LP71 is absent, then the integrated circuit IC7 is not supplied with voltage and the half-bridge invertor HW7 cannot start oscillating.

(15) The eighth exemplary embodiment represented in FIG. 8 has a mains voltage input j80, j81, a filter circuit with a mains voltage rectifier GL8 connected downstream, said filter circuit being connected to the mains voltage input, a step-up convertor HS8 connected to the DC voltage output of the rectifier GL8, an intermediate circuit capacitor C80 arranged in parallel with the output of the step-up converter HS8, and an externally controlled half-bridge invertor HW8, whose input is connected in parallel with the intermediate circuit capacitor C80. The half-bridge invertor HW8 is driven by means of an integrated circuit IC8, which receives its supply voltage via its terminals j82 and j83 and the resistors R80, R81, R82 and R83. Two load circuits which are connected in parallel and designed as resonant circuits are connected to the half-bridge invertor HW8, said load circuits each having a resonance inductor L82 and L83, respectively, a resonance capacitor C81 and C82, respectively, and also a further capacitor C82 and C84, respectively, and an electrodeless discharge lamp LP80 and LP81, respectively. In this case, the supply current for the integrated circuit IC8 does not flow via the two resonance inductors L82, L83, as in the case of the seventh exemplary embodiment, but rather only via the induction coils L81 and L82 of the two electrodeless discharge lamps LP80, LP81. If one of the discharge lamps LP80 or LP81 is absent, then the integrated circuit IC8 is not supplied with voltage and the half-bridge invertor HW8 cannot start oscillating.

(16) The ninth exemplary embodiment of the invention as represented in FIG. 9 has a mains voltage input with the mains voltage terminals j90, j91, a filter and a mains voltage rectifier GL9, a step-up convertor HS9 connected downstream, an intermediate circuit capacitor C90, which is connected to the output of the step-up convertor HS9 and supplies the supply voltage for an invertor HW9. Two load circuits which are connected in parallel and are designed as resonant circuits are connected to the invertor HW9, said load circuits each having a resonance inductor L90 and L91, respectively, capacitors C91, C92 and C93, C94, respectively, and two electrical terminals j92, j93 and j94, j95, respectively, for the at least one induction coil L92 and L93, respectively, of an electrodeless discharge lamp LP90 and LP91, respectively. The invertor HW9 is driven with the aid of a control circuit S9. The respective ignition capacitors C93 and C94 are connected in parallel with the respective terminals j92, j93 and j94, j95. One terminal of the balancing capacitors C91 and C92 is respectively connected to the invertor HW9, while their other terminal is connected to the resonance inductor L90 and L91, respectively, via the tap V90 and V91, respectively. This circuit arrangement additionally has two non-reactive resistors R90, R91, which are each connected to the positive pole of the intermediate circuit capacitor C90, on the one hand, and to the tap V90 and V91, respectively, in the respective load circuit, on the other hand. The taps V90, V91 are furthermore respectively connected to an input of the control circuit S9. The control circuit S9 has a monitoring element which is connected upstream or integrated into the control circuit, said monitoring element being, for example, a logic circuit which monitors the electrical potential at the taps V90 and V91 and forwards a corresponding evaluation signal to the control unit S9. If no lamp LP90, LP91 is connected to the terminals j92, j93 or j94, j95, then the tap V90 or V91, respectively, is at a comparatively high electrical potential essentially determined by the charge state of the intermediate circuit capacitor C90. If, on the other hand, a lamp LP90 or LP91, respectively, is connected to the terminals j92, j93 or j94, j95, respectively, then the tap V90 or V91, respectively, is connected to earth via the respective resonance inductor L90 or L91 and the corresponding induction coil L92 or L93, respectively and the tap V90 or V91, respectively,

is therefore at a comparatively low electrical potential. The monitoring element generates a digital or analogue evaluation signal corresponding to the electrical potential at the tap V90 or V91, respectively, and feeds said signal to the control circuit S9. The control circuit S9 is designed in such a way that it enables the invertor HW9 to start oscillating only when the electrical potential at the taps V90 and V91 falls below a predetermined value prescribed by the dimensioning of the circuit components. This ensures that no ignition attempts are made in the absence of a lamp LP90 or LP91.

(17) The tenth exemplary embodiment represented in FIG. 10 largely corresponds to the ninth exemplary embodiment. The method of operation of the circuit arrangements of these two exemplary embodiments is identical. The resistors R90, R91 have simply been replaced by the equivalent resistors R90' and R91', which are connected to the positive terminal of the intermediate circuit capacitor C90, on the one hand, and to a tap arranged between the resonance inductor and the lamp in the respective load circuit, on the other hand. All the other components correspond to one another. Therefore, the same reference symbols have been used for identical components in FIGS. 9 and 10.

(18) The circuit arrangement of the eleventh exemplary embodiment as represented in FIG. 11 shows the application of the invention to a full-bridge invertor for operating two electrodeless discharge lamps LP110, LP111 connected in parallel. The circuit arrangement according to this exemplary embodiment has, in a manner similar to that described for the first exemplary embodiment, a mains voltage connection, a filter and a mains voltage rectifier and also a step-up convertor, which are not represented in FIG. 11. The terminals j110, j111 shown in FIG. 11 are connected to the output of the step-up convertor, with the result that the intermediate circuit capacitor C109 is connected in parallel with the output of the step-up converter. A full-bridge invertor comprising the switching transistors Q110, Q111, Q112, Q113 and a control circuit (not represented) is connected downstream of the intermediate circuit capacitor C109. Two resonant circuits which are connected in parallel and each have a resonance inductor L110 and L111, respectively, an ignition capacitor C110 and C111, respectively, and a balancing capacitor C112 and C113, respectively, are arranged in the bridge path of the full-bridge invertor Q110, Q111, Q112, Q113. Two electrical terminals j112, j113 and j114, 115 are respectively connected in parallel with the respective ignition capacitor C110 and C111 and serve for the connection of at least one induction coil L112 and L113, respectively, of an electrodeless discharge lamp LP110 and LP111, respectively. Furthermore, the circuit arrangement has a non-reactive resistor R110, which is arranged in parallel with the switching path of the transistor Q 110, and two current leads j116, 117, which connect the control circuit (not represented) of the full-bridge invertor Q110, Q111, Q112, Q113 to a respective tap in one of the bridge paths in each case. Two DC paths are produced in this way, into which are connected, in each case proceeding from the positive pole of the intermediate circuit capacitor C109, the non-reactive resistor R110, the first resonance inductor L110, the terminal j112, the induction coil L112 of the first discharge lamp LP110, the terminal j113 and the first current lead j116, and, respectively, the non-reactive resistor R110, the second resonance inductor L111, the terminal j114, the induction coil L113 of the second discharge lamp LP111, the terminal j115 and the second current lead j117. If one of the discharge lamps LP110 or 111 is absent, then one of these DC paths is interrupted. In that case, the control circuit, which, by way of example, may be designed as an integrated circuit in a manner similar to that in the case of the seventh exemplary embodiment, receives no supply voltage and the full-bridge invertor cannot start oscillating. The circuit arrangement does not make any ignition attempts in that case.

(19) FIG. 12 shows, according to the twelfth exemplary embodiment, the application of the invention to a free-running half-bridge invertor for operating two electrodeless discharge lamps connected in parallel. This circuit arrangement has, in a manner similar to that described for the first exemplary embodiment, a mains voltage connection, a filter and a mains voltage rectifier and also a step-up converter, which are not represented in FIG. 12. The terminals j120, j121 shown in FIG. 12 are connected to the output of the step-up converter, with the result that the intermediate circuit capacitor C120 is connected in parallel with the output of the step-up converter. A half-bridge invertor formed by the two switching transistors Q120, Q121 is connected downstream of the intermediate circuit capacitor C120. Two load circuits which are designed as resonant circuits and are arranged in parallel with one another are connected to the centre tap between the two switching transistors Q120, Q121, said load circuits each having a resonance inductor L120 and L121, respectively, an ignition capacitor C121 and C123, respectively, a balancing capacitor C122 and C124, respectively, and two electrical terminals j122, j123 and j124, j125, respectively, for at least one induction coil L122 and L123, respectively, of an electrodeless discharge lamp LP122 and LP121,

respectively, said electrical terminals being arranged in parallel with the respective ignition capacitor C121 and C123. This circuit arrangement additionally has a non-reactive resistor R120, which is connected to the positive pole of the intermediate circuit capacitor C120, on the one hand, and to the centre tap between the two switching transistors Q120, Q121, on the other hand, and two current leads j126, j127, which in each case connect a tap in the respective load circuit to an input of the control circuit (not represented) of the half-bridge invertor Q120, Q121, said tap being located between the terminal j123 and j125, respectively, and the corresponding balancing capacitor C122 and C124, respectively. The control circuit of the half-bridge invertor Q120, Q121 comprises a transformer (not represented) having a primary winding connected into the load circuit of the half-bridge invertor and two secondary windings which are respectively connected to the control electrode of one of the two switching transistors Q120, Q121, and also a starting circuit which, with the aid of a diac, generates trigger pulses for the control electrode of the switching transistor Q121 in order to enable the half-bridge invertor to start oscillating. Such a free-running half-bridge invertor with such a control circuit is described for example in the German Patent Application with the official file reference 196 50 110.5.

of the transistor Q1 and the emitter terminal of the transistor Q2 or the emitter resistor R5, is arranged in parallel with the smoothing capacitor C3. A load circuit designed as a series resonant circuit is connected to the voltage output, that is to say to the centre tap M, of the half-bridge inverter Q1, Q2. The load circuit has the primary winding N1 of the toroidal-core transformer belonging to the driving apparatus, a coupling capacitor C4, a lamp inductor L5 and a resonance capacitor C6, which are all connected in series. The centre tap M of the half-bridge inverter Q1, Q2 is connected via the primary winding N1, the coupling capacitor C4, the lamp inductor L5 and the resonance capacitor C6 to the anode of the diode D1 and to the junction point j3. The circuit arrangement furthermore has a trapezoidal capacitor C7, whose first terminal is connected to the anode of the diode D1 and to the junction point j3 and whose second terminal is connected to the centre tap M of the half-bridge inverter Q1, Q2. In addition, the circuit arrangement has a starting apparatus comprising a diac DC, a starting capacitor C9, a resistor R7 and a diode D4, and terminals j5, j6, j7, j8 for two series-connected low-pressure discharge lamps LP1, LP2 and an auxiliary ignition capacitor C8. The auxiliary ignition capacitor C8 is arranged in parallel with the second low-pressure discharge lamp LP2. A first terminal of the auxiliary ignition capacitor C8 is connected via a node in the load circuit to the resonance capacitor C6 and to the lamp inductor L5. The second terminal of the auxiliary ignition capacitor C8 is connected to the second electrode of the first low-pressure discharge lamp LP1 and to the first electrode of the second low-pressure discharge lamp LP2. The first electrode of the first low-pressure discharge lamp LP1 is connected via the terminal j5 to the cathode of the diode D1, to the collector of the transistor Q1 and to the positive terminal of the smoothing capacitor C3 and via the terminal j6, the resistor R7 the starting capacitor C9 to the terminal j4 and also to the negative terminal of the smoothing capacitor C3. The second electrode of the second low-pressure discharge lamp LP2 is connected via the terminal j8 to the lamp inductor L5, to the resonance capacitor C6 and to the auxiliary ignition capacitor C8.

(5) After the circuit arrangement has been switched on, the mains

voltage
rectified by the mains voltage rectifier GL is present across the back-up
capacitor C2. The starting capacitor C9 is charged to the breakdown voltage of
the diac DC via the diode D1 and the resistor R7, with the result that the diac
DC generates trigger pulses for driving the base electrode of the transistor Q2
and thereby triggers the initiation of the oscillation of the half-bridge
inverter Q1, Q2. With the aid of the toroidal-core transformer RK, the base
electrodes of the transistors Q1, Q2 are driven in such a way that the
transistors Q1, Q2 switch alternately. After the turn-on of the transistor Q2,
the starting capacitor C9 is discharged via the diode D4, via the switching
path of the transistor Q2 and via the emitter resistor R6 to such an extent
that the diac DC no longer generates further trigger pulses. A high-frequency
alternating current, whose frequency is determined by the switching cycle of
the transistors Q1, Q2, flows through the load circuit and through the
series-connected lamps LP1, LP2. A DC voltage whose value corresponds
approximately to 1.4 times to 1.5 times the peak value of the mains voltage is
built up across the smoothing capacitor C3. The coupling capacitor C4 is
charged approximately to half of the voltage present across the smoothing
capacitor C3. Due to alternate switching of the transistors Q1, Q2, the centre
tap is alternately connected to the negative and to the positive terminal of
the smoothing capacitor C3 and the potential of the centre tap is
correspondingly decreased or increased. As a result, a high-frequency
alternating current determined by the transistor switching cycle flows in the
load circuit. During the switching intermissions of the transistors Q1, Q2,
during which both transistors Q1, Q2 are in the off state, the energy stored in
the lamp inductor L5 maintains the current flow through the corresponding
freewheeling diode D2 and D3, respectively. The lamp inductor L5 forms a
series resonant circuit with the resonance capacitor C6. The electrical
components of the circuit arrangement are dimensioned in such a way that, in
order to ignite a gas discharge in the low-pressure discharge lamps LP1, LP2, a
resonant -increased voltage is provided across the resonance capacitor C6 and
across the auxiliary ignition capacitor C8. After the gas discharge has been
ignited, the series resonant circuit C6, L5 is damped by the impedance of the
discharge paths of the low-pressure discharge lamps LP1, LP2.

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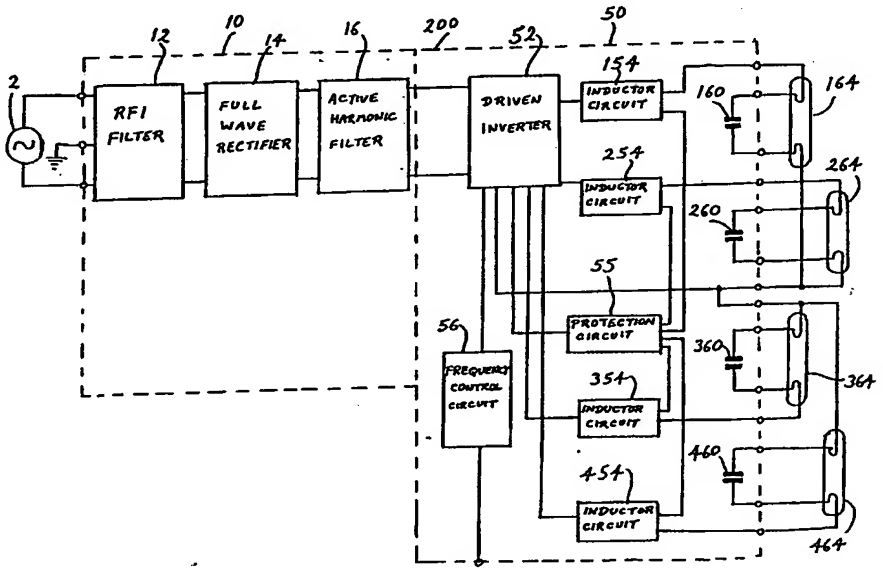
(54) Title: ELECTRONIC BALLAST CIRCUIT FOR GAS DISCHARGE LAMP

(57) Abstract

An electronic ballast circuit for a gas discharge lamp includes a driven inverter (52) the high frequency oscillatory ouput of which is supplied to a gas discharge lamp (164) through a current limited inductor (154) with a capacitor (160) in parallel with the lamp. A protection circuit includes an additional winding (152) on the inductor (154) which monitors the peak voltage and current of the lamp (164). The signal from the additional winding (152) is fed to a threshold detector and latch circuit (170) which operates to remove the drive from the inverter (52) and de-energise the lamp (164) if the voltage across the lamp exceeds a first predetermined value. Additional protection is provided by a voltage clamping circuit (166) which shorts out the additional winding (152) if the voltage across the lamp exceeds a second predetermined value higher than the first before the lamp is de-energised, thereby to damp the resonant circuit of the inductor (154) and capacitor (160). The additional winding (152) also supplies power for a low-voltage stabilised supply for parts of the ballast circuit. The ballast circuit can supply a number of lamps (164, 264, 364, 464) connected in parallel to the driven inverter (52), a respective inductor (154, 254, 354, 454) with additional winding (152, 252, 352, 452), and a respective capacitor (160, 260, 360, 460) being provided for each lamp.



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ELECTRONIC BALLAST CIRCUIT FOR GAS DISCHARGE LAMP

This invention relates to electronic ballast circuits for gas discharge lamps.

Electronic ballast circuits, of the kind comprising an inverter having an oscillatory output for connection to a gas discharge lamp, a current limiting inductor in series with the output of the inverter and a capacitor for connection in parallel with the lamp, are well known. The circuits operate at a frequency at or close to the resonant frequency of the circuit including the current limiting inductor and parallel capacitor, to apply a voltage to the lamp which is high enough to effect ignition. In order to avoid damage to the ballast and/or lamp and unsafe operating conditions, it is necessary to provide protection means for limiting the voltage applied to the lamp.

It is an object of this invention to provide an improved electronic ballast circuit.

This invention consists in an electronic ballast circuit for a gas discharge lamp, the circuit comprising an inverter having an oscillatory output for connection to a gas discharge lamp, a current limiting inductor in series with the output of the inverter, and a capacitor for connection in parallel with the lamp, in which there are provided protection circuit means comprising a monitoring circuit inductively coupled to the current limiting inductor and means for inhibiting the voltage applied to the lamp on receipt of a signal from the monitoring means if the voltage exceeds a predetermined value.

Preferably, the inverter is a driven inverter and the means for inhibiting the voltage applied to the lamp comprises means for

removing the drive from the inverter on receipt of a signal from the monitoring circuit thereby to de-energise the lamp.

In one form of the invention, the monitoring circuit includes an additional winding on the current limiting inductor, and a threshold detector circuit arranged to supply a signal to the inverter if the voltage across the additional winding exceeds a predetermined value.

In accordance with another aspect of the invention, additional protection means are provided to connect the additional winding in a closed circuit if the voltage applied to the lamp exceeds a second predetermined value higher than the first predetermined value, thereby to damp the resonant circuit of the current limiting inductor and parallel capacitor to reduce the voltage applied to the lamp. The additional protection means preferably comprises a voltage clamping circuit connected in parallel with the additional winding.

In accordance with a further aspect of the invention, a low-voltage supply for parts of the circuit is derived from the monitoring circuit inductively coupled to the current limiting inductor.

Suitably, means are provided to control the output frequency of the inverter on switch-on of the circuit so that during an initial preheating period a voltage lower than the striking voltage is applied to the lamp, following which a rising voltage is applied to the lamp until ignition is effected or the protection circuit operates.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of an electronic ballast circuit in accordance with the invention, and

Figure 2 is a circuit diagram of part of the circuit of Figure 1.

Referring to the drawings, the electronic ballast circuit is divided into two sections, a first section 10 referred to hereinafter as the "line conditioner" and a second section 50 referred to hereinafter as the "ballast unit". The two sections are mounted in a common housing 200, provided with suitable terminals by means of which the input of the line conditioner can be connected to a mains supply 2 and the output of the ballast unit can be connected to a number of discharge lamps. In the illustrated embodiment, the circuit supplies four lamps, 164, 264, 364 and 464, though any number of lamps could be connected to the circuit.

The line conditioner 10 comprises a radio frequency interference (RFI) filter 12, a full wave rectifier circuit 14, and an active harmonic filter 16. The RFI filter 12 provides a high impedence to signals at the operating frequency of the driven inverter 52 and active harmonic filter 16, and also provides primary surge protection against mains derived transients. The full wave rectifier circuit 14 provides both AC rectification and secondary mains surge protection, including overvoltage protection for the active harmonic filter 16. The active harmonic filter 16 is used to maintain a near sinusoidal input current from the mains supply 2. This enables the circuit to comply with regulations governing equipment drawing power from the public mains, where these apply. The elements of the line conditioner 10 may be of

generally conventional form and therefore will not be described further.

The ballast unit 50 comprises a driven inverter 52, which is supplied with the smoothed DC output of the line conditioner 10. The high frequency output of inverter 52 is supplied via an inductor circuit 154 and a capacitor 160 to the lamp 164. In addition, the driven inverter 52 receives inputs from a frequency control circuit 56 and a protection circuit 55.

Additional inductor circuits 254, 354 and 454, and capacitors 260, 360 and 460 respectively are provided to supply the output of the inverter 52 to the lamps 264, 364 and 464, a common return for the lamps being provided through line 53.

The circuit of the ballast unit 50 is shown in more detail in Figure 2. For convenience, only one lamp 164 is shown connected to the circuit in Figure 2. The driven inverter 52 is a conventional half-bridge formed by capacitors 66 and 68, power MOSFETs 62 and 64, and transformer 70. The gate electrodes of transistors 62 and 64 are voltage clamped by zener diodes 63 and 65 and are connected to the secondary windings 72 and 74 of the transformer 70, the primary winding 76 of which is connected to output terminals of the integrated circuit 78.

The integrated circuit 78 includes components forming parts of the frequency control circuit 56 and protection circuit 55. The remaining components of the frequency control circuit are provided by resistors 80, 82, 84 and 86, transistor 100, capacitor 106 and diode 88. The

circuit is arranged to provide an initial pre-heat period, preferably greater than 400ms, during which a sufficiently high pre-heating current flows through the lamp. On switch-on of the ballast circuit the capacitor 106 begins to charge through resistors 84 and 86, from a low-voltage supply, which is provided through transistor 110 as described below. The transistor 102 is therefore rendered conducting, placing resistor 80 in parallel with resistor 82. This has the effect of increasing the frequency of the signal applied to the primary 76 of transformer 70 and therefore the operating frequency of the driven inverter. Since the impedance of the inductor circuit 154 at this higher frequency is greater, the combination of the higher frequency in conjunction with inductor circuit 154 determines the preheating current of the heater electrodes of lamp 4. The value of the parallel capacitor 160 is chosen so as to prevent the parallel combination of inductor circuit 154 and capacitor 160 from being sufficiently close to resonance at the higher frequency, thereby preventing the generation of a high voltage which would otherwise appear across the lamp and ignite it.

As the capacitor 106 charges, the voltage at the base of transistor 100 falls until the transistor is rendered non-conducting. When capacitor 106 is fully charged, any residual current flow due to leakage from the capacitor is diverted via resistor 86, effectively preventing transistor 100 from conducting. The frequency of the driven inverter is now solely determined by the resistor 82.

The transition between the two states is not instantaneous, and transistor 100 operates in the linear mode for a period of times. The frequency of the driven inverter decreases over this period, so that the parallel combination of the inductor 154 and parallel capacitor 160 moves towards resonance, thereby gradually increasing the voltage across the lamp 164, until it reaches a sufficient voltage to cause the lamp to ignite.

The protection circuit 55 includes an additional winding 152 on the inductor circuit 154. One terminal of the winding 152 is connected to ground whilst the other is connected through diode 153 and resistors 156 and 158 to the input of threshold detector and latch circuit 170. The input is also connected to ground through resistor 157, across which is connected capacitor 159. The output of the latch circuit 170 is connected to the integrated circuit 78.

The junction of resistors 156 and 158 is connected to the collector of transistor 110 forming part of a stabilised low-voltage supply, as described below. The base of the transistor 100 is connected to ground through zener diode 162, and a reservoir capacitor 164 is connected between the collector of transistor 110 and ground.

A voltage clamping circuit 166, which may comprise a zener diode, a voltage-dependent resistor or any other suitable device, is connected in parallel with capacitor 164.

The winding 152 effectively monitors the peak lamp voltage and current. The voltage across the winding 152 is fed to the threshold sensing and latch circuit 170 via the voltage divider formed by resistors 157 and 158. If the voltage applied to circuit 170 exceeds a

predetermined value, a latch is activated, and the output voltage supplied to integrated circuit 78 rises, causing the output to transformer 70 to be turned off, removing the drive to the inverter and de-energising the lamp. The circuit is arranged so that the latch circuit 170 will be actuated if the voltage applied to the lamp 164, after the preheating period, rises to a value (typically in the region of 1200 volts) above that at which the lamp is expected to ignite. The latch circuit 170 includes a reset circuit to reset the circuit and enable the lamp to be re-started after it has been switched off.

The capacitor 159 in parallel with resistor 157 prevents the latch circuit 170 responding to spurious transient voltages in the circuit. The slight delay thus introduced may in some circumstances allow the voltage applied to the lamp to increase above the predetermined value before the lamp is de-energised. This may occur for example when an additional lamp is connected to the ballast circuit whilst it is operating, so that the additional lamp is not subjected to the preheating current. In some countries, statutory regulations set an absolute maximum for the voltage which may be applied to the lamp. To ensure that the voltage cannot exceed such a limit, additional protection is provided by the voltage clamping circuit 166. This is set to conduct if the voltage at the junction of resistors 156 and 158 exceeds a value corresponding to the maximum voltage to be applied to the lamp. Conduction of the device 166 effectively short-circuits the additional winding 152, damping the resonant circuit formed by inductor 154 and capacitor 160 and reducing the voltage applied to the lamp 164.

The transistor 110 and associated components provide a stabilised low-voltage supply for various control circuits, including the protection circuit 55 and frequency control circuit 56, the power for the low-voltage supply being drawn from the additional winding 152, and from the additional windings on the other inductor circuits 254, 354 and 454, if lamps are connected to those circuits.

It will therefore be appreciated that the use of an additional winding on the current limiting inductor, in accordance with the invention, to monitor the peak lamp voltage and current has the advantage of enabling three functions to be performed, namely monitoring the peak voltage and current to enable the lamp to be shut down if a predetermined threshold is reached, providing a voltage clamp to prevent the lamp voltage exceeding a maximum permissible level, irrespective of other circuit conditions, and providing power for low voltage control circuits of the ballast.

It will be appreciated that modifications can be made in the described embodiment. For example, in an alternative form of the invention, the protection circuit may be arranged to increase the frequency of the output of the driven inverter, to reduce the voltage applied to the lamp, instead of removing the drive to the inverter as in the described embodiment.

CLAIMS

1. An electronic ballast circuit for a gas discharge lamp, the circuit comprising an inverter having an oscillatory output for connection to a gas discharge lamp, a current limiting inductor in series with the output of the inverter, and a capacitor for connection in parallel with the lamp, in which there are provided protection circuit means comprising a monitoring circuit inductively coupled to the current limiting inductor and means for inhibiting the voltage applied to the lamp on receipt of a signal from the monitoring means if the voltage exceeds a predetermined value.

2. A circuit as claimed in Claim 1, in which the inverter is a driven inverter and the means for inhibiting the voltage applied to the lamp comprises means for removing the drive from the driven inverter on receipt of a signal from the monitoring circuit, thereby to de-energise the lamp.

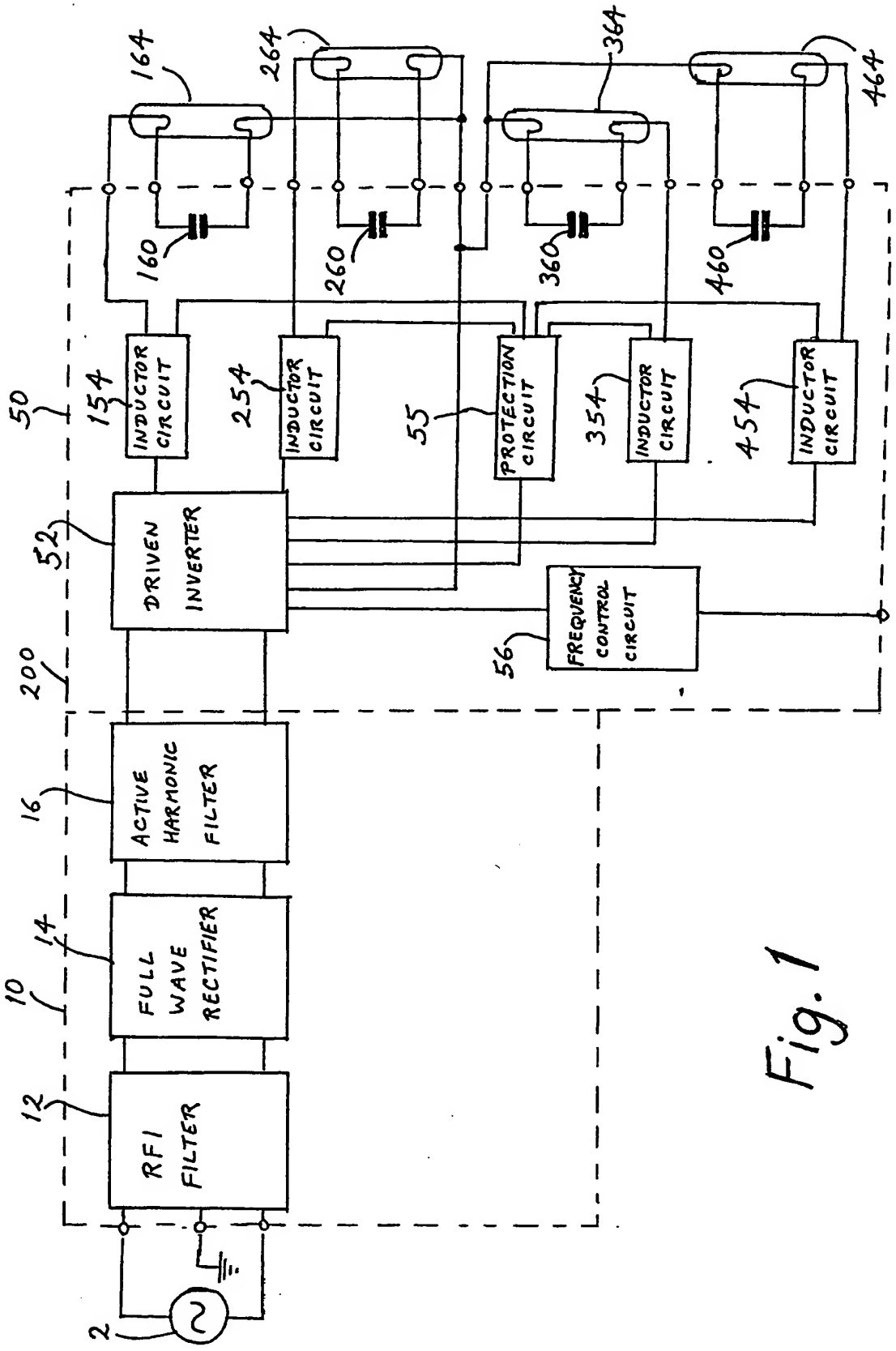
3. A circuit as claimed in Claim 1 or Claim 2, in which the monitoring circuit includes an additional winding on the current limiting inductor, and a threshold detector circuit arranged to supply a signal to the inverter if the voltage across the additional winding exceeds a predetermined value.

4. A circuit as claimed in Claim 3, in which additional protection means are provided to connect the additional winding in a closed circuit if the voltage applied to the lamp exceeds a second predetermined value higher than the first predetermined value, thereby to damp the resonant circuit of the current limiting inductor and parallel capacitor to reduce the voltage applied to the lamp.

5. A circuit as claimed in Claim 4, in which the additional protection means comprises a voltage clamping circuit connected in parallel with the additional winding.

6. A circuit as claimed in any preceeding claim, in which a low-voltage supply for parts of the circuit is derived from the monitoring circuit inductively coupled to the current limiting inductor.

7. A circuit as claimed in any preceding claim, in which means are provided to control the output frequency of the inverter on switch-on of the circuit so that during an initial preheating period a voltage lower than the striking voltage is applied to the lamp, following which a rising voltage is applied to the lamp until ignition is effected as the protection circuit operates.


164
264
364
464
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260
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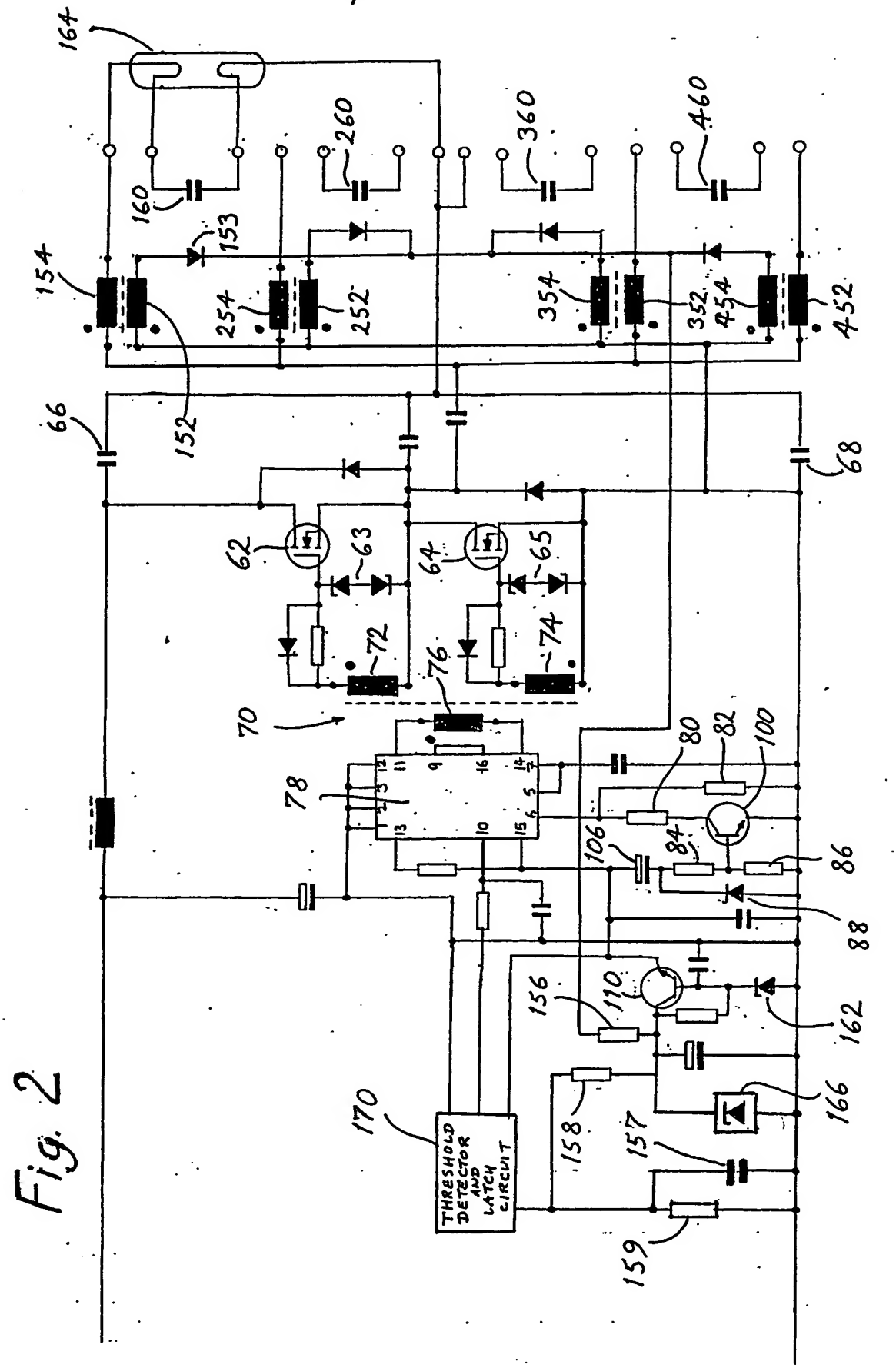
460
50
154
INDUCTOR CIRCUIT
254
INDUCTOR CIRCUIT
55
PROTECTION CIRCUIT
354
INDUCTOR CIRCUIT
454
INDUCTOR CIRCUIT
52
DRIVEN INVERTER
56
FREQUENCY CONTROL CIRCUIT
200
16
ACTIVE HARMONIC FILTER
14
FULL WAVE RECTIFIER
10
12
RFI FILTER
2

Fig. 1


164
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170
THRESHOLD DETECTOR AND LATCH CIRCUIT

Fig. 2

I. ERNATIONAL SEARCH REPORT

International Application No PCT/GB 89/00438

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 4 H05B41/29

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 4	H05B ; H02M

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category ?	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X	EP,A,059064 (THORN EMI) 01 September 1982 see the whole document	1-7
X	WO,A,8201276 (THOMAS INDUSTRIES) 15 April 1982 see page 11, line 15 - page 13, line 35; figures 1, 3	1-3, 6, 7
A	DE,A,3432266 (KNOBEL) 21 March 1985 see the whole document	1-7
A	WO,A,8302537 (MINITRONICS) 21 July 1983 see page 4, line 17 - page 7, line 11; figure 2	1-5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19 JUNE 1989	29. 06. 89
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	SPEISER P.

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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